TPS65161EVM-194

The TPS65161EVM-194 takes an 8-V to 14-V input rail and provides the four bias supply voltages that are typically required for TV monitors and TFT LCD panels. Specifically, the TPS65161EVM-194 has one boost converter with integrated low-side FET, one buck converter with integrated high-side FET, one positive charge pump controller, and one negative charge pump controller, each requiring external Schottky diodes. Supporting passive components for the boost and buck converter include inductors and capacitors. Supporting passive components for the charge pumps include capacitors.

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1 Introduction

This section contains background information for the TPS65161EVM-194 evaluation module (EVM).

1.1 Specification

Table 1 provides a summary of the TPS65161EVM-194 performance specifications. All specifications are given for an ambient temperature of 25°C:

Table 1. Performance Specification Summary

Specification	Voltage Range (V)			Current Range (mA)		
	Min	Typ	Max	Min	Typ	Max
V_{IN}	11.4	12	12.6	5000		
V_S	17.5	18	18.6			1300
V_{GL}	–5.2	–5	–4.8		50	135 (1)
V_{LOGIC}	3.15	3.3	3.32			2300
V_{GH}	30.6	32 (2)	33.1		50	75 (3)

(1) VGx droops 3% at this output current. Because the charge pumps are driven from V_S, increasing their output current decreases the maximum available output current from V_S. These measurements were taken assuming no external load on V_S.
(2) Assumes that SUP = V_S.
(3) VGx droops 3% at this output current. Because the charge pumps are driven from V_S, increasing their output current decreases the maximum available output current from V_S. These measurements were taken assuming no external load on V_S.

1.2 Modifications

The primary goal of this EVM is to facilitate user evaluation of the TPS65161EVM-194 IC that powers a typical large TFT display. To facilitate user customization of the EVM, the board is designed with devices having 805 or larger footprints. An actual implementation would likely occupy less total board space.

1.2.1 Customizing the Power Supply

Users can change each rail's regulated output voltage by changing the appropriate feedback resistors as listed in the data sheet (SLVS617). The user is responsible for not exceeding each outputs maximum voltage specifications in the data sheet. In addition, alternate capacitors, inductors, and/or diodes can be used. When using alternate capacitors, ensure that the minimum recommended capacitance listed in the data sheet is used and that the capacitor voltage rating is appropriate. The switching converters are designed to be used with ceramic output capacitors. Using nonceramic output capacitors with significantly large equivalent series resistance (ESR) can result in larger output ripple or unstable operation from the inductive switching converters. Each charge pumps' flying and output capacitors must be ceramic output capacitors. When selecting an alternate inductor, use the data-sheet design equations to ensure that the appropriate inductance value is selected and that the inductor's current rating is appropriate for desired output current. Using an inductor with a higher rated current allows each inductive switcher to provide more output current and a higher rated input supply may be required. However, using an inductor with larger dc resistance results in lower efficiency. When using alternate diodes, ensure that the diode is rated for both the expected peak current and power design equations.

Changing the value of C3 on the SS pin changes the soft-start time of the boost converter. The buck converter soft-start time is fixed. To change the start-up delay time between the buck converter and the negative charge pump, change capacitor C5 on the DLY1 pin. To change the start-up delay time between the buck converter reaching regulation and the boost converter and positive charge pump starting, change capacitor C4 on the DL2 pin.

1.2.2 Input-to-Output Isolation

The nonsynchronous boost converter has a path from input to output (i.e., V_{IN} to V_S). In addition, if the positive-charge-pump, high-side diode (D4D6) is tied to V_S, the path continues to the output of the positive charge pump (V_{GH}). The TPS65161 provides a gate drive (GD) pin that controls an external PMOS FET switch and supporting passives in order to provide input-to-output isolation. Pin GD is an open-drain output and is latched low when the boost converter is within 8% of its nominal regulated output voltage. GD goes high impedance when EN2 is taken low. The MOSFET (Q1) and supporting passives (C23, C26, R12, and R15) are not populated on the EVM, and switch Q1 is shorted by a zero-ohm resistor (R13). The bill of materials provides recommended values for these components in the event the user desires to add them.

1.2.3 Implementing Short-Circuit Protection for the Charge Pumps

The positive charge pump circuit providing VGH does not have internal short-circuit protection. If short-circuit protection is desired, replace zero-ohm resistor R2 with the resistor having the value computed in the following equation:

$$R2 = (V_S - V_{SCHOTTKY})/I_{SC\text{-}VGH}$$

Where $I_{SC\text{-}VGH}$ are the desired short-circuit current levels for each charge pump. Note that the maximum output current will be limited to approximately $I_{SC\text{-}VGH}/2$.

2 Setup and Test Results

This section explains the input, output, and jumper connections of the TPS65161EVM-194. It also provides guidance on how to set up test equipment for evaluating the EVM and provides test results.

2.1 Connections and Jumpers

The DEFAULT jumper settings are required for the EVM to operate within the specifications of Table 1.

J1 – VGH IN This jumper is used to connect the positive charge pump's high-side external diode either before (OS) or after (VS) the input-to-output isolation MOSFET (Q1). J1 must be installed but because the isolation MOSFET is shorted out on the EVM, placing J1 in either position yields the same results. If Q1 is installed, it is recommended that J1 be placed to VS so that the positive charge pump also has input-to-output isolation.

J2 – EN2 The middle pin of this jumper connects to the enable pin of the boost converter and positive charge pump. When EN2 is connected to VIN, the boost converter and positive charge pump starts up after the buck converter is within regulation and the delay time set by DLY2 has passed. When EN2 is connected to GND, the boost converter and positive charge pump are disabled. The EN2 pin must be connected to either VIN or GND and not left floating.

J3 – EN1 The middle pin of this jumper connects to the enable pin of the buck converter and negative charge pump. When EN1 is connected to VIN, the buck converter starts up and, after a delay time set by DLY1, the negative charge pump starts up. When EN1 is connected to GND, the buck converter and negative charge pump are disabled. The EN1 pin must be connected to either VIN or GND and not left floating.

J4 – FREQ The middle pin of this jumper connects to the FREQ pin of the IC. When FREQ is connected to VIN, the switching frequency is 750 kHz. When FREQ is connected to GND, the switching frequency is 500 kHz. The FREQ pin must be connected to either VIN or GND and not left floating. The DEFAULT connection is FREQ that is connected to 750 kHz (VIN).

J5 – VIN and GND The input supply positive and ground return connections must be connected to J5.

J6 – VGL and GND This header provides the output voltage and ground return connections for the negative charge pump.

J7 – V_LOGIC and GND This header provides the output voltage and ground return connections for the buck converter.

J8 – VGH Boost The middle pin of this jumper connects to output pins of the J10. When this jumper is connected to 2X, the charge pump's external transfer diode (D4D6) is connected to J10 (VGH output header) which results in the charge pump operating as a voltage doubler. When this jumper is connected to 3X, the transfer diode is connected to an additional charge pump stage (D4-D7, C17, C16). If the resistor divider is appropriately modified, the charge pump operates as a voltage tripler. The DEFAULT connection is VGH connected to 2X.

J9 – VGH and GND This header provides the output and ground return connections for the positive charge pump.

J10 – VS and GND This header provides the output and ground return connections for the main boost converter.

J11 – SUP The middle pin of this jumper connects to the SUP pin, which provides drive to both charge pumps. In most applications, SUP must be connected to OS to allow the highest possible voltage on the positive charge pump. Because the SUP pin is rated only for a maximum of 15 V, SUP must be connected to V_{IN} when V_S is greater than 15 V. The DEFAULT connection is SUP connected to OS.

2.2 Recommended Test Setup

Connect at minimum a 5-A rated power supply set to provide 12 V ± 5% to J5. Do not exceed 15 V on J5. Operation at an input voltage down to 8 V is possible, although maximum output current levels will decrease. The output voltages can be monitored by voltmeters and/or an oscilloscope with standard high-impedance voltage probes.

Before enabling the device jumpers using J2 and J3, the user must ensure jumpers J4, J8, and J11 are in their default positions. When EN1 is connected to VIN using J3, the buck converter starts up and, after a delay time set by DLY1, the negative charge pump starts up. When EN2 is connected to VIN using J2, the boost converter and positive charge pump start up after the buck converter is within regulation and a delay time set by DLY2 has passed. The output voltages reach their respective regulation voltages (see Table 1) after the appropriate soft-start times and relative delays. Resistive or electronic loads can be attached to each outputs header (J6 for VGL, J7 for VLOGIC, J8 for VGH, and J10 for VS). Loading each output more than specified in Table 1 results in the output voltage falling out of regulation.

2.3 Test Results

Below are test results using the TPS65161EVM.

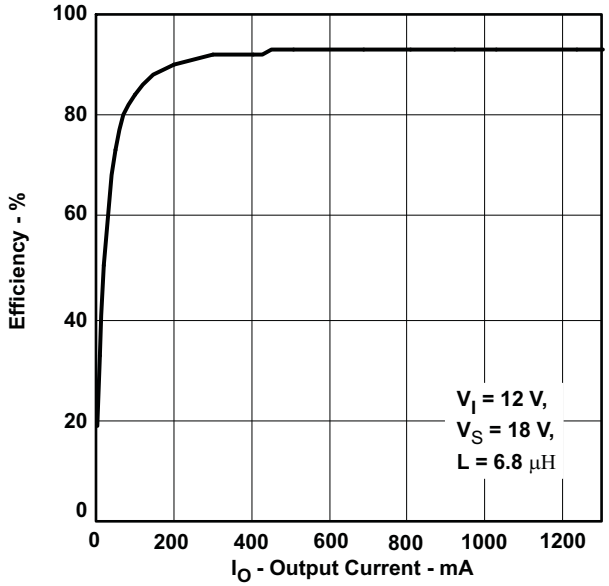

Figure 1. Boost Converter Efficiency

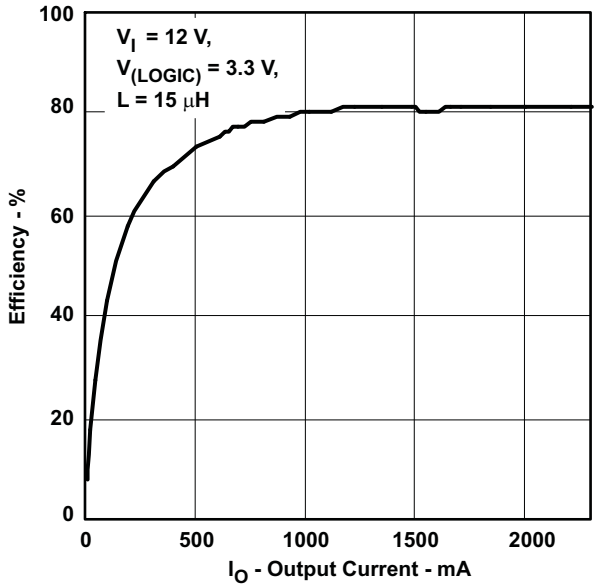

Figure 2. Buck Converter Efficiency

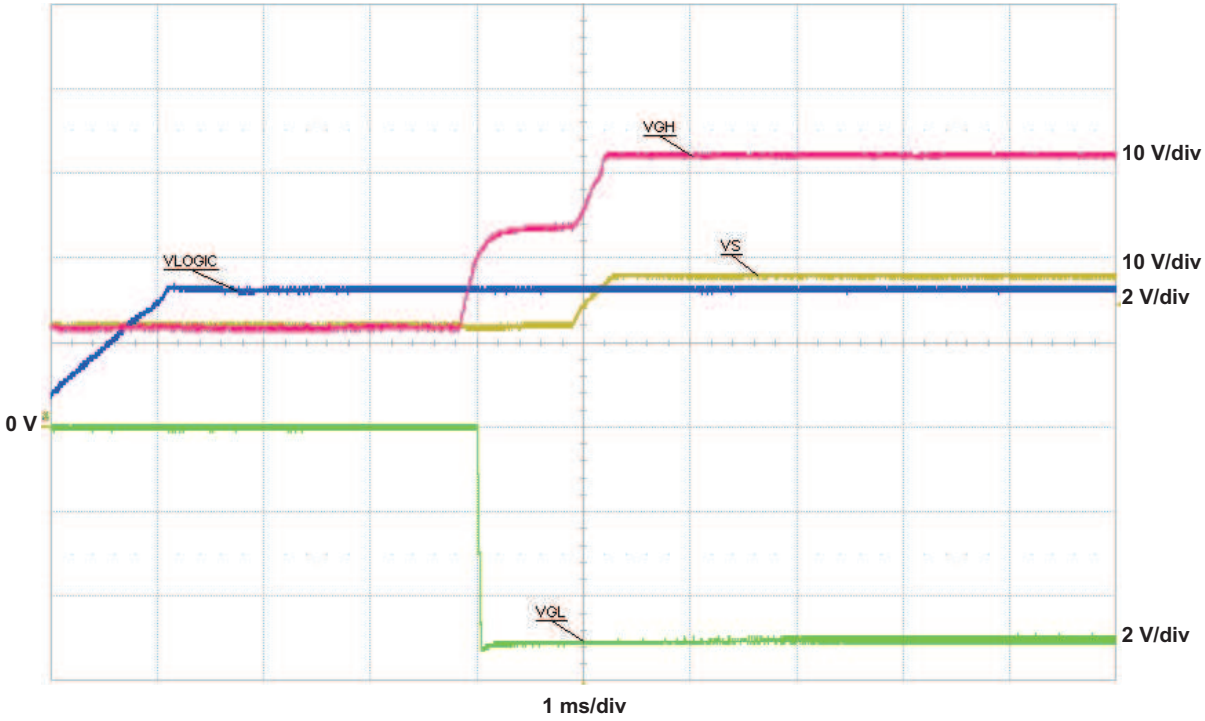

Figure 3. Power-Up Sequencing With EN2 = V_{IN}

3 Board Layout

This section provides board layout recommendations as well as illustrations of the EVM board layers.

3.1 Board Layout Recommendations

The PCB layout is an important step in the power supply design. Poor layout can cause converter instability, load regulation problems, noise, and EMI issues. Especially with a switching dc-dc converter at high load currents, PCB traces that are too thin can cause significant voltage spikes and good grounding becomes important. If possible, it is recommended to use a common ground plane to minimize ground shifts between analog (GND) and power ground (PGND). The following design guidelines are highly recommended when designing a TPS65161-based power supply:

1. Separate the power supply traces for AVIN and VINB, and use separate bypass capacitors.
2. Use a short and wide trace to connect the OS pin to the output of the boost converter.
3. Use short traces for the charge pump drive pins (DRN, DRP) of VGH and VGL because the traces carry switching waveforms.
4. Place the charge pump flying capacitors as close as possible to the DRP and DRN pin.
5. Place the charge pump Schottky diodes as close as possible to the IC respectively to the flying capacitors connected to the DRP and DRN.
6. Route the feedback network of the negative charge pump away from the drive pin traces (DRN) of the negative charge pump This avoids coupling into the feedback network. Use the FREQ pin and trace to isolate DRN from FBN.
7. Place the inductive switching converters Schottky diodes as close to the SW pin as possible in order minimize switching spikes.

The EVM follows these recommendations.

3.2 Board Layers

The following pages show the top assembly and top and bottom layers of the TPS65161EVM-194.

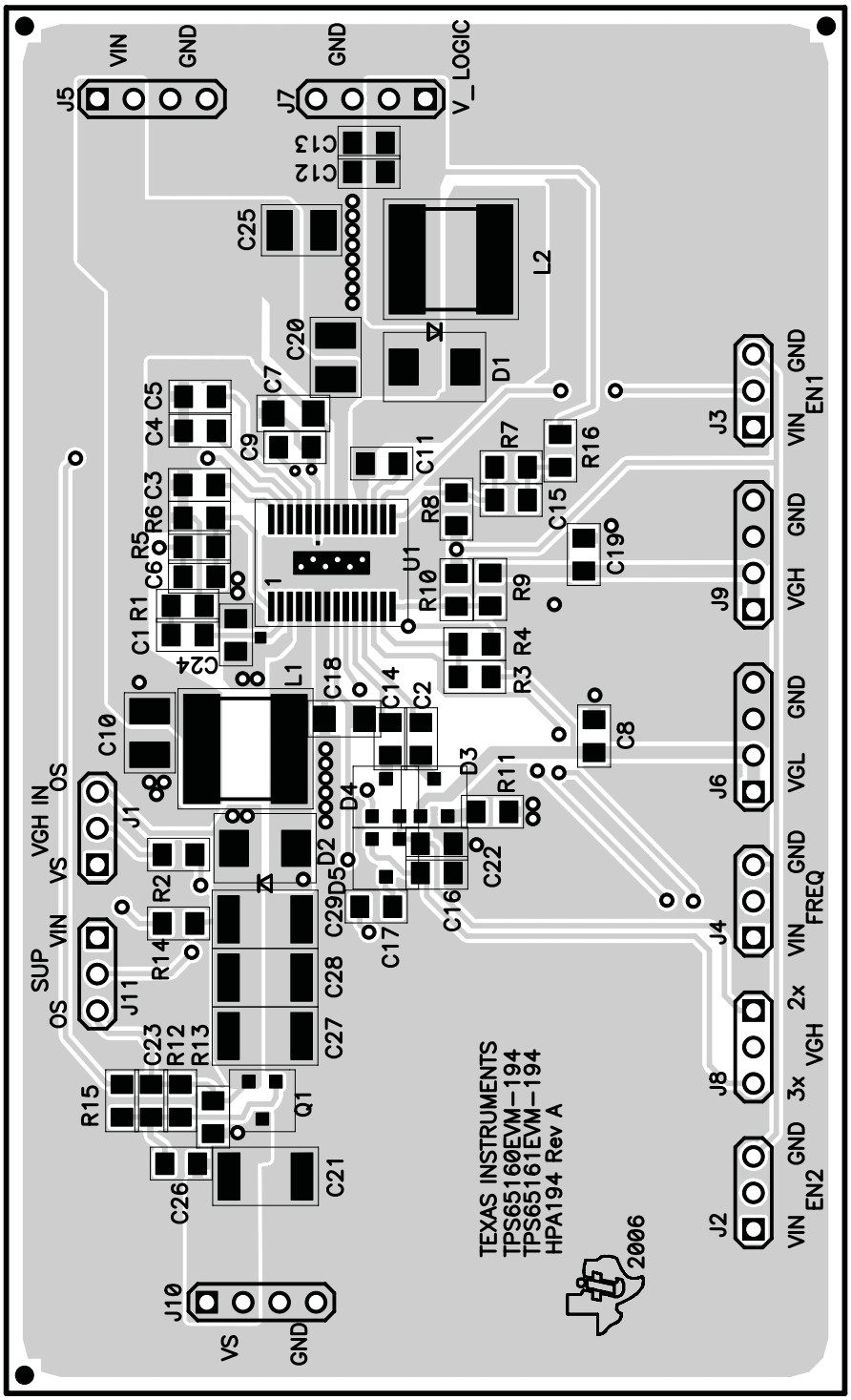

Figure 4. Top Assembly Layer

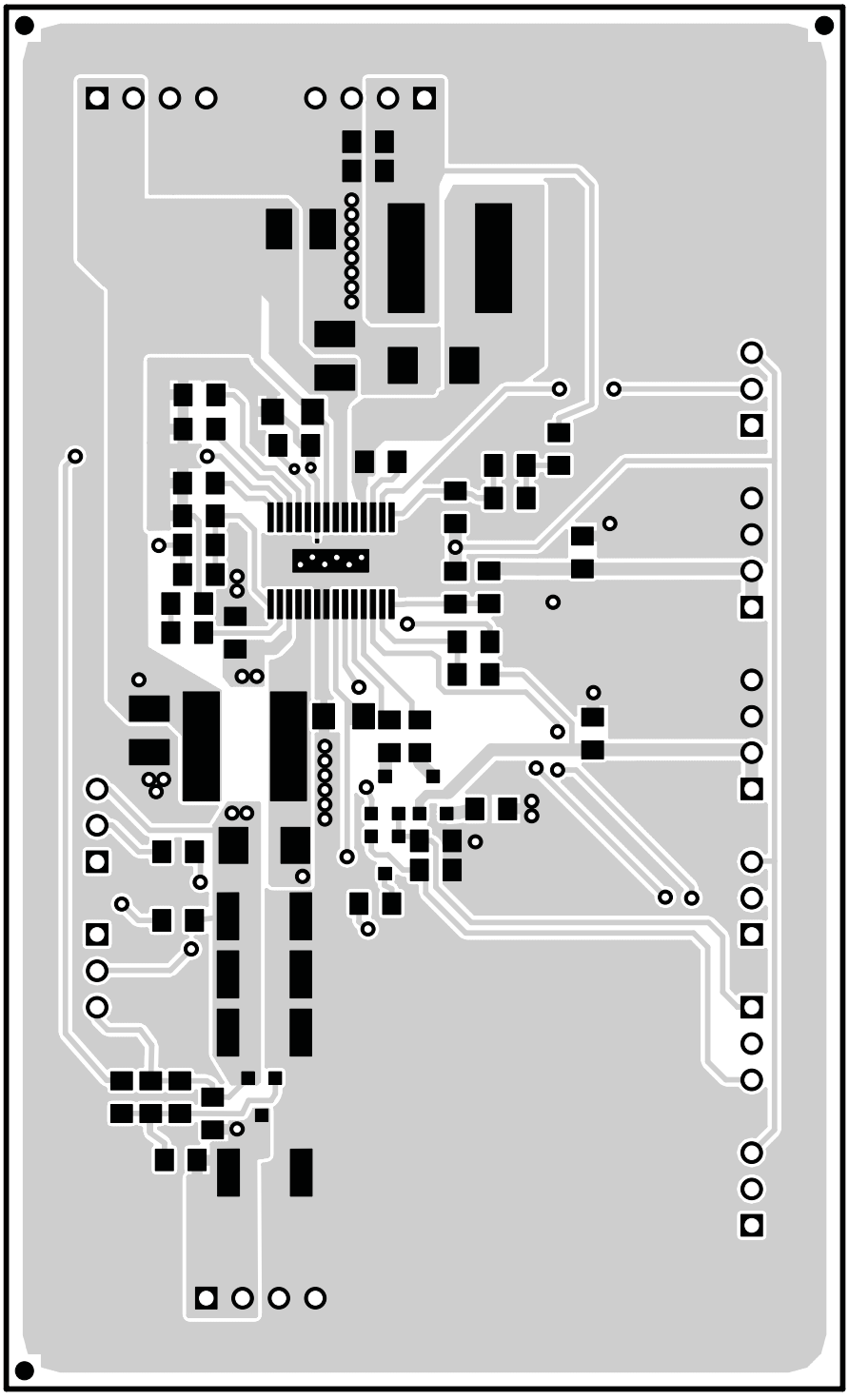

Figure 5. Top Layer

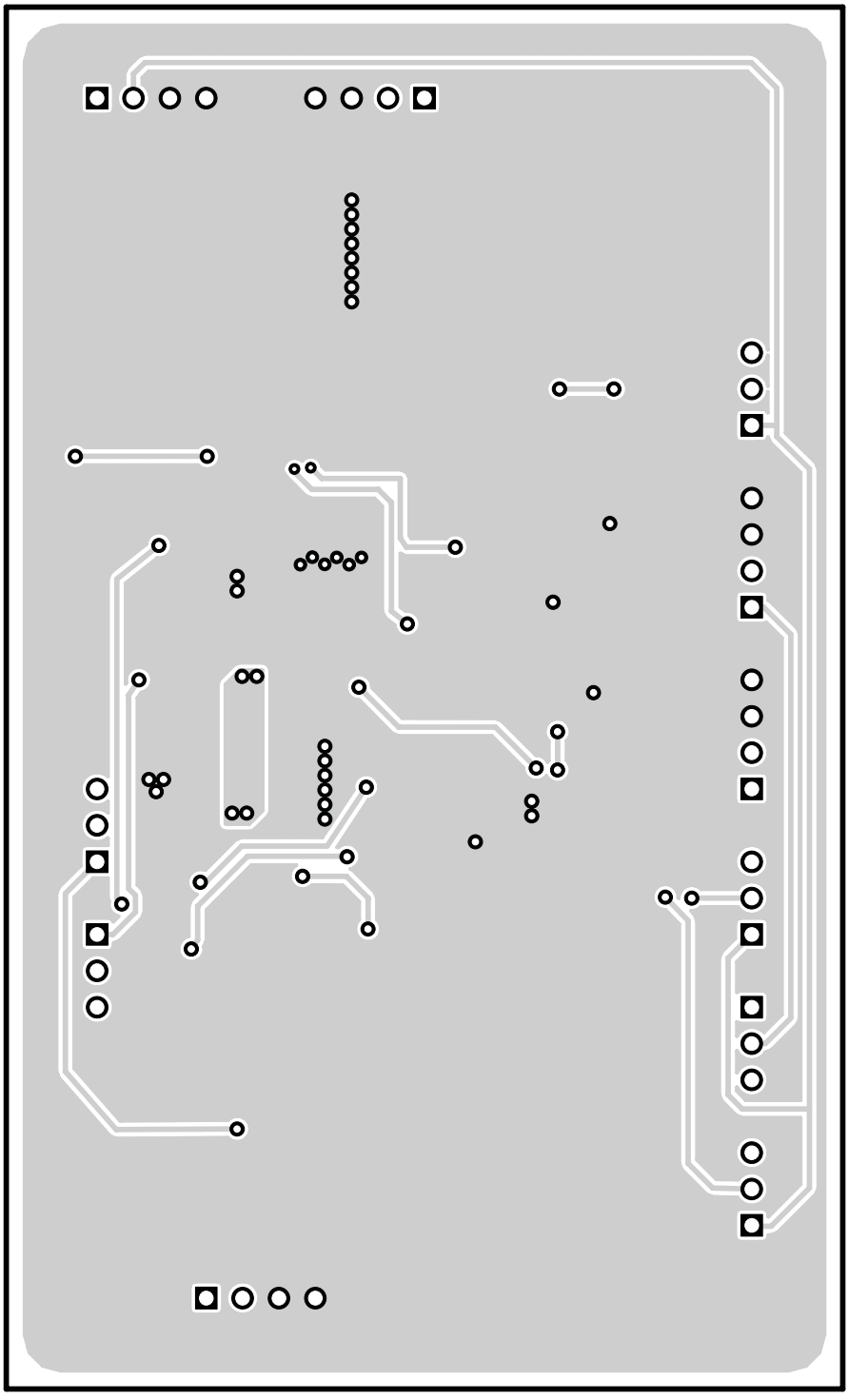

Figure 6. Bottom Layer

4 Schematic and Bill of Materials

This section provides the TPS65161EVM-194 schematic and bill of materials.

4.1 Schematic

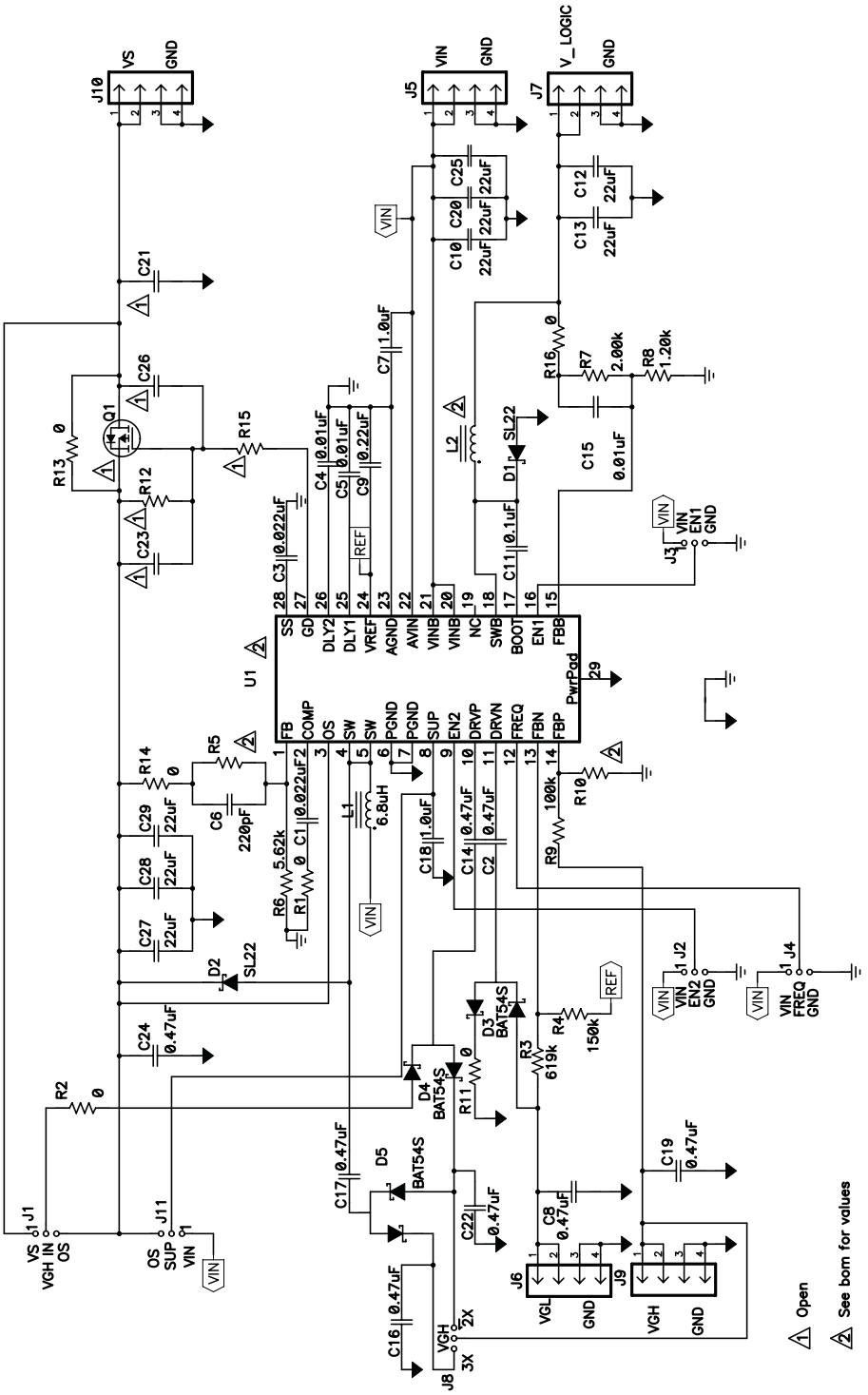

Figure 7. TPS65161EVM-194 Schematic

4.2 Bill of Materials

Table 2. Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
2	C1, C3	0.022µF	Capacitor, Ceramic, 50V, X7R,	0805	UMK212BJ223KD-T	Taiyo Yuden
3	C10, C20, C25	22µF	Capacitor, Ceramic, 16V, X5R, 20%	1210	EMK325BJ226MM-T	Taiyo Yuden
1	C11	0.1µF	Capacitor, Ceramic, 50V, X7R, 10%	0805	UMK212BJ104KG-T	Taiyo Yuden
2	C12, C13	22µF	Capacitor, Ceramic, 6.3V, X5R, 20%	0805	JMK212BJ226MG-T	Taiyo Yuden
7	C2, C8, C14, C16, C17, C19, C22, C24	0.47µF	Capacitor, Ceramic, 35V, X5R, 10%	0805	GMK212BJ474KG-T	Taiyo Yuden
1	C14	0.47µF	Capacitor, Ceramic, 50V, X7R, 10%	0805	GRM21BR71H474KA88L	Murata
0	C21	Open	Capacitor, Ceramic, xxV	1812		
0	C23, C26	Open	Capacitor, Ceramic, xxV	0805		
3	C27, C28, C29	22µF	Capacitor, Ceramic, 16V, X5R, 20%	1812	EMK432BJ226MM-T	Taiyo Yuden
3	C4, C5, C15	0.01µF	Capacitor, Ceramic, 50V, X7R, 10%	0805	GRM216R71H103KA01	Murata
1	C6	220pF	Capacitor, Ceramic, 50V, C0G, 5%	0805	Std	Std
2	C7, C18	1.0uF	Capacitor, Ceramic, 35V, X7R, 10%	1206	GMK316BJ105KL-T	Taiyo Yuden
1	C9	0.22µF	Capacitor, Ceramic, 50V, X5R, 10%	0805	UMK212BJ224KG-T	Taiyo Yuden
2	D1, D2		Diode, Schottky Rectifier, 2A, 20 V	DO-214AA	SL22	Vishay
3	D3, D4, D5		Diode, Dual Schottky, 200mA, 30V	SOT23	BAT54S	Zetex
6	J1, J2, J3, J4, J8, J11		Header, 3 pin, 100mil spacing, (36-pin strip)	0.100 × 3	PTC36SAAN	Sullins
5	J5, J6, J7, J9, J10		Header, 4 pin, 100mil spacing, (36-pin strip)	0.100 × 4	PTC36SAAN	Sullins
1	L1	6.8µH	Inductor, SMT, 2.5A, 44mΩ		7447789006	WUERTH
1	L2	15µH	Inductor, SMT, 2.7A, 50mΩ	10.2 × 3.6	MSS1038-153NX	Coilcraft
0	Q1	Open	MOSFET,P-ch, –30 V, 4 A, 51 mΩ	SOT23		
6	R1, R2, R11, R13, R14, R16	0	Resistor, Chip, 1/10W, 1%	0805	Std	Std
0	R12, R15	Open	Resistor, Chip, 1/10W, 1%	0805		
1	R3	619k	Resistor, Chip, 1/10W, 1%	0805	Std	Std
1	R4	150k	Resistor, Chip, 1/10W, 1%	0805	Std	Std
1	R5	82.5k	Resistor, Chip, 1/10W, 1%	0805	Std	Std
1	R6	5.62k	Resistor, Chip, 1/10W, 1%	0805	Std	Std
1	R7	2.00k	Resistor, Chip, 1/10W, 1%	0805	Std	Std
1	R8	1.20k	Resistor, Chip, 1/10W, 1%	0805	Std	Std
1	R9	100k	Resistor, Chip, 1/10W, 1%	0805	Std	Std
1	R10	3.92k	Resistor, Chip, 1/10W, 1%	0805	Std	Std
1	U1		IC, Bias Power Supply for TV and Monitor TFT LCD Panels	PWP-28	TPS65161PWP	TI
1	--		PCB, 3.8 In × 2.5 In × 0.062 In		HPA194	Any
6	--		Shunt, 100mil, Black	0.100	929950-00	3M

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 8 V to 14 V and the output voltage range of -40 V to 20 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 125°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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